Keynote Lunch Address

"3D Technology Trends & Key Manufacturing Challenges"

Presented by Amandine Pizzagalli – Yole Développement

12:15 – 12:45 - Exhibits Hall

Keynote Abstract

Three-dimensional (3D) technology utilizing Through-Silicon-Via (TSV) interconnects is considered today to be one of the most advanced technologies enabling multifunctional integration. It also brings added value with package form factor reduction and enhancement of electrical performance. 3D technology is not limited to CMOS scaling, it is rather based on enabling various heterogeneous integration by stacking multiple and different type of devices such as Memory, Logic, Analog, MEMS and passive components. It brings more complexity with respect to process technologies but also opens a new path for the evolution of semiconductor packaging technology.

Indeed, emerging platforms using vertical integration with TSV technology, such as 3D/2.5D platforms, have gained significant interest from several companies across the supply chain. Moreover, it has generated the start of the "Middle-End" area, which is supported by several organizations from IDMs to fabless, OSATs, foundries and packaging houses, as well as equipment and material suppliers. The entire supply chain in the packaging industry is evolving, leading to more opportunities for collaboration in order to overcome the remaining technical issues that the industry is currently facing. Lithography, temporary bonding & de-bonding processes, inspection and metrology tools, wafer testing, as well as thermal management are the remaining challenges of this technology.

This work addresses the key technical trends and challenges in lithography for Advanced Packaging. Steppers will become mandatory for TSV packaging due to very tight pitch between bumps. Future needs of 20 µm micro-bumping capabilities and achieving better resolution for Via middle below 2 µm and for very high-level wiring density at the RDL level are being set. Wafer warpage, as one of the key constraints for FO WLP applications is also addressed. Furthermore, temporary bonding and debonding, a key technology for handling extremely thin TSV wafers is analyzed.

In order to address 3D technology requirements and solve the remaining challenges, optimized processes are needed and strong investment has to be made in new design tools and high performing materials. To fulfil 3D needs, the motivation to introduce new manufacturing tools has driven the introduction of equipment coming from the Front-End and Back-End areas to the Middle-End area. This has created competition between Front-End and Back-End equipment vendors, both of which desire market share in the "Middle-End". A trade-off between performance and cost will be needed for the processes that have applications in both front and back-end.

To support the miniaturization trend, front-end tools are preferred for achieving more aggressive features. However, they are typically more expensive. On the other side, back-end equipment generally exhibits lower cost, but can face scaling issues when semiconductor ICs continue to reduce in chip and feature size. In conclusion, the supply chain interaction and key players in the packaging area will be addressed.

Biography

Amandine Pizzagalli is a Technology & Market Analyst at Yole Développement in Lyon France. She is responsible for the Equipment & Material fields for the Advanced Packaging & Manufacturing team at Yole. Amandine graduated as an Engineer in Electronics, with a specialization in Semiconductors and Nano Electronics Technologies. Previously, she worked at Air Liquide with an emphasis on CVD and ALD processes for semiconductor applications.