TSV Impact on Chip Package Interaction (CPI) for 20nm Silicon

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Purpose

• Chip package interaction (CPI) has garnered tremendous interest in advanced technology nodes mainly due to
  – Introduction of low-K (LK) and ultra-low-K (ULK) material in the back end of line (BEOL) and
  – Cu pillar in chip-package interconnect

• Emerging packaging solutions pose additional challenges to CPI
  – 3D integration using through silicon via (TSV) technology
  – New process flow and materials used

• This presentation highlights GLOBALFOUNDRIES’s activity in CPI study on 3D 20nm silicon which includes
  – CPI test structure design,
  – BEOL process control and characterization, and
  – assembly process optimization and reliability tests.

• The key CPI challenges/risks were identified, analyzed and mitigated through DOE studies.
Outline

• Introduction
• CPI challenges in emerging packaging integrating solutions
• CPI test structure design
• BEOL strength tests
  – Dual cantilever beam (DCB)
  – Modified edge lift-off test (MELT)
• Packaging solution and construction
• Assembly process optimization
• Environmental stress tests
• Summary and discussion
Introduction

• Moore’s law has continuously driven the semiconductor industry to scale down device and their interconnects to achieve
  – Higher density and performance, and
  – Low power consumption.

• New materials, processes, and designs for BEOL must be developed to meet these requirements.

• A major area of concern is the intrinsic weakness in the mechanical properties of the ULK dielectrics, and the increase in the number of BEOL metal layers.

• Cu pillar has been used to replace lead-free solder to achieve fine pitch chip-packaging interconnect which exerts more stress in the ULK layer.
3D Package – 20nm Technology BEOL Stack

- A major on-going effort of which is to implement ULK dielectric materials ($k < 2.7$) into Cu interconnects to reduce the RC delay and cross talk.

<table>
<thead>
<tr>
<th>Film</th>
<th>Modulus</th>
<th>Hardness</th>
<th>Adhesion</th>
</tr>
</thead>
<tbody>
<tr>
<td>ULK 2.55</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>LK 2.7</td>
<td>1</td>
<td>1.2</td>
<td>1.3</td>
</tr>
</tbody>
</table>

CPI Challenges in 20nm Technology

- Delamination in ULK layers
  - CTE mismatch
  - Higher stress on ULK layers due to CuP

CPI Challenges in 3D Package

- **TSV impact on BEOL**
  - Doming effect observed after TSV chemical mechanical polishing (CMP) process
  - Decreases metal 1 thickness thereby increasing its resistance
TSV Impact on Metal 1 and Metal 2 – Test Structure

• M1 and M2 serpentines are aligned orthogonally.
• Reference structure is required with no TSV underneath to provide baseline.
• TSV impact is determined by measuring kelvin resistance and leakage between M1 and M2.

![Diagram showing TSV impact on Metal 1 and Metal 2 with Serpentine with TSV underneath and Reference Serpentine.]
TSV Impact on Metal 1 and Metal 2 – Characterization

- Electrical test: Measure serpentine resistance
- Physical cross-section: Observe M1 thickness at center and edge of TSV.

<table>
<thead>
<tr>
<th>Die No.</th>
<th>Doming Height (nm)</th>
<th>M1 Thickness (nm)</th>
<th>Resistance</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>71.66</td>
<td>46.63</td>
<td>204.37</td>
</tr>
<tr>
<td>2</td>
<td>22.05</td>
<td>76.1</td>
<td>206.95</td>
</tr>
<tr>
<td>3</td>
<td>74.41</td>
<td>43.42</td>
<td>203.28</td>
</tr>
<tr>
<td>4</td>
<td>79.37</td>
<td>46</td>
<td>233.69</td>
</tr>
<tr>
<td>5</td>
<td>71.93</td>
<td>47.63</td>
<td>233.08</td>
</tr>
<tr>
<td>6</td>
<td>52.92</td>
<td>45</td>
<td>239.22</td>
</tr>
<tr>
<td>7</td>
<td>52.92</td>
<td>46.2</td>
<td>222.82</td>
</tr>
<tr>
<td>8</td>
<td>74.41</td>
<td>52.59</td>
<td>238.79</td>
</tr>
<tr>
<td>10</td>
<td>49.61</td>
<td>72.93</td>
<td>181.11</td>
</tr>
<tr>
<td>11</td>
<td>85.99</td>
<td>41.2</td>
<td>254.63</td>
</tr>
<tr>
<td>12</td>
<td>49.61</td>
<td>62.13</td>
<td>226.91</td>
</tr>
<tr>
<td>13</td>
<td>66.15</td>
<td>51.1</td>
<td>199.78</td>
</tr>
</tbody>
</table>
TSV Cu Pumping

- Copper pumping in via-middle TSV can affect the BEOL, reducing reliability and possibly shortening device lifetime.
- Caused by copper recrystallization and grain growth during high-temperature processes in BEOL.
CPI Test Structure Design

- CPI test chip to address different failure modes in BEOL, interconnect, and package, including BEOL delamination, dicing induced cracking, CuP fatigue failure, etc.

- Test structures were wired out to CuP interconnect and routed to BGA I/O pins through the package substrate for electrical measurement during reliability testing.

<table>
<thead>
<tr>
<th>CPI Structure</th>
<th>Failure Mode Detection</th>
<th>Chip Location</th>
</tr>
</thead>
<tbody>
<tr>
<td>Perimeter Line</td>
<td>Dicing related Crack Failure</td>
<td>Chip Perimeter</td>
</tr>
<tr>
<td>Delamination Sensor</td>
<td>Corner Delamination</td>
<td>Corner &amp; Center</td>
</tr>
<tr>
<td>Under Bump Crack Sensor</td>
<td>Delamination under bump</td>
<td>Corner &amp; Center</td>
</tr>
<tr>
<td>Via Chain</td>
<td>BEOL Delamination</td>
<td>Corner &amp; Center</td>
</tr>
<tr>
<td>Serpentines</td>
<td>Corrosion / Extrusions</td>
<td>Corner &amp; Center</td>
</tr>
<tr>
<td>CuP Stitch/ Daisy Chain</td>
<td>CuP-Package integrity</td>
<td>Corner &amp; Peripheral</td>
</tr>
<tr>
<td>TSV Stitches</td>
<td>Thinner BEOL</td>
<td>Chip Center</td>
</tr>
<tr>
<td>Wide I/O Daisy Chain</td>
<td>Assembly related Failure</td>
<td>Chip Center</td>
</tr>
</tbody>
</table>
BEOL Strength Evaluation

- 20nm uses advanced ULK film with 2.55 K-value for high performance, which has porous and brittle structures.

- BEOL strength tests
  - Nano-indentation: Capacitive or electrostatic force actuation causes small indent in sample and depth sensing to obtain structural properties such as modulus and hardness.
  - 4 point bending test: Energy release rate $G_c$ as measure of the fracture toughness of materials / interfaces.
  - Dual cantilever beam (DCB)
  - Modified edge lift-off test (MELT)

Dual Cantilever Beam (DCB)

- BEOL strength comparison between TSV and non-TSV wafers.
  - Samples were prepared for the DCB test with vertical stripe orientation (prp-A) and horizontal stripe orientation (prp-B).
  - Default DCB sample prep was used, with Teflon release layer, underfill epoxy, no additional adhesion layer (no SiN), and no surface etching.
  - Stripe size 2.44mm x 70mm.
  - An upper cut-off value for crackstop-$G_c$ of 80J/m² is used in the data evaluation.
Adhesion Analysis – DCB

• Average crackstop-$G_c$ of both wafers are $>20\text{J/m}^2$.

<table>
<thead>
<tr>
<th>#</th>
<th>Sample ID</th>
<th>$G_c$</th>
<th># CS</th>
<th>Wafer Info</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>77MX</td>
<td>66.2</td>
<td>8</td>
<td>With TSVs</td>
</tr>
<tr>
<td>02</td>
<td>75MX</td>
<td>52.3</td>
<td>6</td>
<td>Without TSVs</td>
</tr>
</tbody>
</table>

• Profilometer scans were made to analyze the surface profile after DCB
  - crack deflection towards the surface was observed for structures with $G_c>20$.  

![G_c Probability Distribution](image1.png)

![Profilometer Scan](image2.png)
Modified Edge Lift-off Test (MELT)

- Si substrate coated with ULK layer (thin film) of interest.
- Epoxy as polymer backing layer of thickness (~100µm) was used as a stress-generating layer.
- The sample is subjected to thermal quenching which leads to delamination events due to the thermal coefficient mismatch between the polymer and substrate.
Adhesion Analysis – MELT

- Average $K_{app} > 0.25 \text{MPa m}^{1/2}$ for both wafers.

<table>
<thead>
<tr>
<th>#</th>
<th>Sample ID</th>
<th>$K_{app}$ [MPa m$^{1/2}$]</th>
<th>$D K_{app}$</th>
<th>$T_{c}$ [deg]</th>
<th>Wafer Info</th>
</tr>
</thead>
<tbody>
<tr>
<td>01</td>
<td>77MX</td>
<td>0.29</td>
<td>0.02</td>
<td>-100</td>
<td>With TSVs</td>
</tr>
<tr>
<td>02</td>
<td>75MX</td>
<td>0.27</td>
<td>0.04</td>
<td>-85.6</td>
<td>Without TSVs</td>
</tr>
</tbody>
</table>

- For both type of wafers start point of delamination was within the layer and no systematic differences between the processes observed.
Debonding.

Thermal/Room Temp

Heated vacuum chuck

Flipping and mounting to dicing tape and dicing
Stealth dicing through the tape from backside

Die attach and Underfilling

Die attach and Underfilling of Top die

Pad finish

Die attach and Underfilling

Assembly approach

Internal Device Build-up

- Package cross-sectional view

- CPI test vehicle information

<table>
<thead>
<tr>
<th>Package type</th>
<th>FcCSP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Package (mm)</td>
<td>14x14x0.76</td>
</tr>
<tr>
<td>CPI chip size (mm)</td>
<td>11 x 11</td>
</tr>
<tr>
<td>Bottom Die I/Os</td>
<td>3290</td>
</tr>
<tr>
<td>Top Die I/Os</td>
<td>1751</td>
</tr>
<tr>
<td>Bump pitch (µm)</td>
<td>80</td>
</tr>
<tr>
<td>Substrate size (mm)</td>
<td>14 x 14</td>
</tr>
<tr>
<td>Substrate Layer</td>
<td>2/2/2</td>
</tr>
</tbody>
</table>

Package - Topside

Package - Bottomside
Environmental Stress Test

- Electrical readouts are performed at regular intervals to monitor package reliability during the various environmental stress steps.

<table>
<thead>
<tr>
<th>Stress Test</th>
<th>Conditions</th>
<th>Electrical Readout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pre-conditioning (MSL3)</td>
<td>24 hrs. @ 125°C 192 hrs. soak @ 30ºC/60% RH 260ºC reflow x3</td>
<td>Pre-conditioning readout</td>
</tr>
<tr>
<td>High Temperature Storage (HTS)</td>
<td>150ºC</td>
<td>Readout @ 250 hrs. Readout @ 500 hrs. Readout @ 750 hrs. Readout @ 1000 hrs.</td>
</tr>
<tr>
<td>Unbiased Highly Accelerated Stress Test (uHAST)</td>
<td>130ºC/85% RH</td>
<td>Readout @ 96 hrs. Readout @ 192 hrs.</td>
</tr>
<tr>
<td>Thermal Cycling (TC)</td>
<td>-55ºC to 125ºC</td>
<td>Readout @ 250 cycles Readout @ 500 cycles Readout @ 750 cycles Readout @ 1000 cycles</td>
</tr>
</tbody>
</table>
Early Reliability Analysis

- Packages with both 100um and 260um thick top-die

<table>
<thead>
<tr>
<th>Readout Rel. Stress</th>
<th>Sample Size</th>
<th>Precon</th>
<th>96</th>
<th>250</th>
<th>500</th>
<th>750</th>
<th>1000</th>
</tr>
</thead>
<tbody>
<tr>
<td>TCB</td>
<td>387</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pass/Tested: 247/247</td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td></td>
<td>Readout expected on 4/12</td>
</tr>
<tr>
<td>uHAST</td>
<td></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pass/Tested: 53/53</td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>HTS</td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td>Readout expected on 3/30</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pass/Tested: 115/117</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- FA is ongoing for TCB500 fails.
Summary and Discussion

- CPI risk due to the introduction of ULK layers in BEOL was mitigated through DOE studies to control the moisture absorption rate.

- Additional challenges to CPI in emerging packaging solutions were addressed through process optimization
  - Doming effect due to TSV CMP process: CMP dishing to prevent thinner M1 on top of TSV.
  - TSV Cu pumping: Either through extended single anneal step or double anneal step.

- GLOBALFOUNDRIES’s activity in CPI study on 3D 20nm silicon by demonstrating
  - BEOL strength analysis on TSV wafers which are comparable to non-TSV wafers,
  - Exposed die solution for better heat dissipation, and
  - Low environmental stress fails during early reliability analysis.
Thank you

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