Advanced Packaging Concepts for Manufacturing

Homi Dalal, Ph.D.

Consulting Engineer
e-mail: hormazdalal@aol.com

ABSTRACT

IC package manufacturing spans from micro miniature implants to Peta-flops supercomputer; the common theme is *smaller, lighter, cheaper* and *performance compliant* products. There is a myriad of factors affecting these four driving forces; however, single most important controlling factor is 'Interconnection'; whether it is on-chip, between chips, to board, between boards or between systems. IC packaging has so far mostly used electrical interconnects; wire bond, solder bumps, copper pillars, thin film interconnects and Through Silicon Vias (TSV) are used in first level packaging; Pin Through Holes (PTH), Surface Mount Technology (SMT) and Connectors are used in second level packaging. However, the increasing clock speed and wiring density inside systems require replacement of electrical interconnections with optical interconnections, just like the optical fiber which took over the task of long distance communications from electrical cables.

The second most important factor in IC packaging is ' process technology'; the same interconnect technology can be accomplished using different process technologies; for example, bumping can be achieved by 'Parallel Processing' like stencil printing or by 'Discrete Processing' like individual solder ball deposition technique. The low throughput of 'Discrete Processing' can be alleviated by the advancements in laser, optical and electro-mechanical (robotic) techniques. Most tools make use of 'Data Control' to some degree; a tool designed with proper Data Control, robotics and optical or laser controls, produces higher synergy in production and thereby, lowest cost of yielded product.

A pragmatic approach to analysis of advanced packaging technologies to meet the future needs of commercial products will be presented.

INTRODUCTION

With the shipment of the first commercially available information processing machine, IBM System/360, exactly fifty years ago provided us with a technology to build a smarter planet by retrieving, storing, transporting and transforming via binomial digits, raw data into usable information and knowledge. The theme in these past five decades has been *smaller, lighter, faster* and *cheaper* products. One of the most effective ways to simultaneously provide

improvements in these four measurements has been to provide increased integration. For example, System/360 had separate cabinets for logic and memory components; the logic function was provided by an array of discrete transistor packages and memory function was provided on magnetic drums. With the invention of RAM technologies to hold charge in tiny capacitors, a memory function could be obtained using the silicon transistors. Both, memory and logic, devices could then be monolithically formed. In the past fifty years, such function-integration, monolithic or not, has been the most effective driving force in 'system miniaturization' from mainframe through work stations, laptop, and smart phones to smart watches. Apart from form-factor reduction, miniaturization has also provided performance improvements and reduced assembly processing steps which in turn manifested into higher yield, easier testability and cost reduction.

APPROACH & DESCRIPTION

A system may be divided into three parts[1]:

IC chips and packages (Data processors);
Modules (electrical, mechanical and optical sub systems); and,
System components (passives; antenna; power source; thermal management; and, system interconnections).

The advancement in IC chips has broadly followed Moore's law for increase in device density and clock speed at regular interval of time. Major contributors in satisfying Moore's law have been photolithography, copper interconnect with double damascene process[2], low-k interlevel dielectric and high-k gate dielectric; nevertheless, advancements in tools, specifically stepper photo tools, have been the major technology enablers. These IC technology advancements have been complimented by advancements in IC package interconnect technologies like high speed high density wirebonding or bumping; and advancements in packaging technologies like leadframe, flip chip, wafer level, interposer, stacked die and stacked packages.

The package to card interconnection has seen one major transformation, from Pin Through Hole to Surface Mount Technology (SMT). Some heavier parts still need to use Pin Through Hole. In module arena, although the assembly of discrete function components is still widely used, the integration of electrical-mechanical functions (MEMS) or electrical-optical functions (optoelectronics) or mechanical-optical functions have been in production and rapidly gaining more applications. In systems' arena, effort has been mostly made on power supply, thermal management, ease of component diagnostic and replaceability.

Overall, the components density in ICs has increased 6 fold in the past 50 years whereas components density at system level has increased 2.5 fold. The focus for system

miniaturization, should, therefore, be on system integration and system scaling[1]. For small size systems, e.g., Cardiac Implant with Remote Monitoring, Wafer Level Packaging could provide a solution (Fig. 1). For larger systems or use of heterogeneous components, an interposer technology (Fig. 2) will provide a complete solution. The availability of high Q and integrated passives in WLP makes this a more attractive packaging technology. Through Silicon Vias (TSV) and Through Package Vias (TPV) would provide added miniaturization.

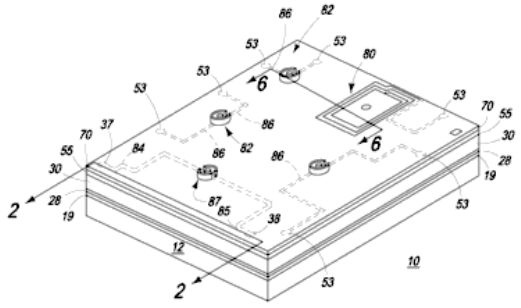

Fig. 1: Dalal, et al, US patent no. 8,129,266

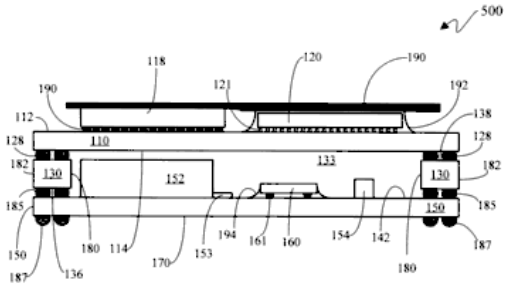

Fig. 2: Dalal, et al, US patent no. 6,618,267

3.0 NANO TECHNOLOGY

Nano technology provides materials with unusual properties. Copper film with extra fine nanometer size grains is imminent. Such fine grain materials have 10X higher yield strength than ED copper, etching of ultra-narrow lines is feasible, voids and hence open lines will be far reduced, and, nano-via will be more reliable than the present day micro-via. On chip or on substrate decoupling capacitors will be possible using nano-grain ultrathin void-free TaN film. Selective coating of RF components with non-conducting nano-carbon tubes will provide efficient EMI shielding. Most of all, high thermal conductivity of nano thermal interface material will help reduce thermal resistance by 200X.

THERMAL

Thermal generation coming from Power dissipation has been a perennial problem. Interconnects at every level is a major and growing contributor of power dissipation. These interconnects have predominantly been electrical interconnects. The resistive part of the electrical interconnects, augmented by skin effect, not only cause signal propagation loss and heat generation, but it also limits density of data (bits/sec) that can be transmitted. The major focus in high speed multi band data transmission systems is therefore on replacing the electrical wiring with optical interconnects[3].

CONCLUSIONS

Apart from reducing the thermal management burden, optical interconnects will help with system miniaturization by removing bulky cable harnesses at the system level, and provide increased data transmission capacity with improved signal integrity.

Those materials and processes will prevail that have less manufacturing cost. Batch processes provide the least cost where it is possible; however, robotic technologies may make the data-driven assembly of individual parts more attractive.

In conclusion, future trend is system level packaging using wafer level packaging or interposers, and miniaturization using optical-interconnects and nano materials.

REFERENCES

1. Rao R. Tummala, "Changing Role Packaging", PowerPoint PPT presentation, *www.powershow.com*
2. Dalal, et al, "Copper Interconnections", *U.S. Patent no. 6,348,731.*
3. David A. Miller, "Device Requirements for Optical Interconnects to Silicon Chips", *Proc. IEEE, July 2009, pp1166-1170.*