TSV Impact on Chip Package Interaction for 20nm Silicon

Sukeshwar Kannan, Shan Gao, Rahul Agarwal, Daniel Smith, Luke England
GLOBALFOUNDRIES US Inc.
400 Stonebreak Road Extension, Malta, NY 12020 USA

Sukeshwar Kannan – E-Mail: Sukeshwar.kannan@globalfoundries.com

Abstract

Chip packaging interaction (CPI) has garnered tremendous interests in advanced technology nodes mainly due to the introduction of low-K (LK) and ultra-low-K (ULK) material in the back end of line (BEOL) and Cu pillar in chip-package interconnect [1]. In addition to these advances in the silicon technology nodes emerging packaging integrating solutions like 3D integration using through silicon via (TSV) technology are expected to pose additional CPI challenges and risk due to new process flow and materials used. This paper presents GLOBALFOUNDRIES's activity in CPI study on 3D 20nm silicon which includes CPI test structure design, BEOL process control and characterization, and assembly process optimization and reliability tests. The key CPI challenges/risks were identified, analyzed and mitigated through DOE studies.

As with standard 2D flipchip packaging, warpage due to overmolding plays a crucial part in overall CPI reliability for 3D packages as well. Experiments were completed with various encapsulating mold compounds (EMC), molding configuration, and top die thickness to minimize package warpage. Package level reliability evaluation was performed on all DOE splits, with results clearly showing that an exposed top die solution is optimum for warpage control. In addition to reduced warpage and improved CPI performance, the exposed top die results in better thermal dissipation. Full experimental descriptions and results are provided.